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| EXAMINER | |
|---|---|
| ENGLUND, TERRY LEE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/761,239 | CHOI, JONG-HYUN | |
| | Examiner | Art Unit | |
| | Terry L. Englund | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *Jan 22, 2004 & May 12, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-26 and 29-37* is/are rejected.

7)☒ Claim(s) *4,7,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05122005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Drawings*

The drawings are objected to because the three memory blocks labeled with "MB0" in Fig. 5 should be re-identified as --MB0--, --MB1--, and --MBy-- as cited on page 13, lines 1-2. Fig. 8 should have the information within parenthesis behind "ND22" of Fig. 8 either clarified, or removed from the figure. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

The title "Semiconductor Integrated Circuit Device" of the invention is not descriptive since it is considered generic. A new title is required that is clearly indicative of the invention to which the claims are directed. For example, the following title is suggested: --Level shifting circuit with thick and thin gate MOS transistors--.

The disclosure is objected to because of the following informalities: Page 7, line 7 "NM1" should be --MN1--. Page 9, line 6 of paragraph 0028 "MP2" should be --MP3--. Page 11, last line "MN13" should be --MN12--. Page 13, line 6 of paragraph 0036 "DRA1k[0:x} should be --DRA1y[0:x]--. Page 14, line 5 of paragraph 0038 "outputs" should be --output--. Page 16, line 1 of paragraph 0043 "DRA0k" should be --DRAk0--. Page 18, line 6 "ND24" and line 10 "ND23" are both believed to mean –ND22--. Page 19, line 2 of paragraph 0048 "DRA10" should be --DRAi0--; and --is open-- should be added after the first occurrence of "ND22" on line 4 of the same paragraph. Lines 6-8 of paragraph 48 on page 19 needs clarification to which node and which transistors are actually being discussed. For example, was "node ND22 is transmitted through NMOS transistor MN24" meant to be --node ND24 is transmitted through PMOS transistor MP24--? Page 21, line 2 of paragraph 0056 "P25" should be --MP25--. Appropriate corrections are required.

### *Claim Objections*

The numbering of claims 34-36 is not in accordance with 37 CFR 1.126 since claim "34" occurs twice, and each occurrence has a different limitation. When claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). In this case, the second

occurrence of original claim "34" should have been numbered as --35--, and originally numbered claims "35" and "36" should have been numbered as --36-- and --37--, respectively.Therefore, for purposes of this Office Action, the four originally numbered claims 34, 34, 35, and 36 will be referred to as claims 34, 35, 36, and 37, respectively.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5-6, 8-18, 21, 23-31, 34, and 36-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The "connection node of the second and third MOS transistors" limitation is misleading, and/or inaccurate in each of claims 5 and 8. For example, unless --the first and third MOS transistors-- was meant within each of claims 5 and 8, which of the applicant's figures actually shows an inverter coupled to a node of the second/third MOS transistors as recited? It is not clear how "a voltage higher than the power supply voltage" within each of claims 6 and 9 relates to "a first voltage higher than a power supply voltage" as recited within claim 1. Since the power terminal of claim 10 receives "a first high voltage", and the first transistor's source is coupled to "the first high voltage", it is not understood if the "power terminal" and the "source" are actually coupled in common? The use of "a second low voltage" in claim 10, line 8 implies a first low voltage which has not been clearly identified. For example, is the "power supply voltage" of claim 10, line 3 meant to be considered the first low voltage? Similar to claims 5 and 8 above, the "connection node of the second and third transistors" limitation is misleading, and/or inaccurate in claim 15. Therefore, was --first and

third transistors-- meant? It is not clear how "a voltage higher than the power supply voltage" within claim 16 relates to "a first high voltage that is higher than a power supply voltage" as recited within claim 10. The use of "a second low voltage" in claim 23, line 2 implies a first low voltage which has not been clearly identified. Claim 25, line 1 "the first MOS transistor" is believed to be misleading, and/or inaccurate. Was --the fifth MOS transistor-- meant instead? Using the applicant's Fig. 4 as an example, fifth/sixth transistors MN11/MN12 are controlled by an inverted input signal with respect to one another, wherein first transistor MP5 is controlled by the voltage on node ND3. Since claim 29 indicates each row decoder and driver circuit includes a fifth internal node, it is not clear in claim 30 if a single inverter is coupled to only one of the apparent plurality of fifth internal nodes from claim 29, or if a corresponding inverter is coupled to its own respective fifth internal node. Similarly, which "word line" does the "inverter" actually drive, since each row decoder/driver circuit has its own corresponding word line? It is not clear how "a voltage higher than the power supply voltage" within claim 31 relates to "a first high voltage higher than a power supply voltage" as recited within claim 19. The operating voltage of the third MOS transistor within claim 34 is confusing. For example, if the transistor is actually operating at the first voltage, how can it also operate at the second voltage as claim 34 apparently implies? Since both original claims 35 and 36, now renumbered as claims 36 and 37, depend on "claim 34", it is not clear which one of the two original claims 34 (now renumbered as 35 and 36, respectively) is meant.

Claim 21 recites the limitation "the second low voltage" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 29 recites the limitation "the row decoder and driver block" in line 2 with insufficient antecedent basis for this limitation in the claim. Was claim 29 meant to depend on claim 28?

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 10-13, and 32-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Hardee. Figs. 1 and 2 each show a circuit device comprising first internal circuit 12 including first MOS transistor 12 operating at a first voltage VCCP higher than power supply voltage VCC (e.g. see column 1, lines 39 and 49); second internal circuit 16 including second MOS transistor 16 operating at a second voltage (i.e. ground) lower than first voltage VCCP; and restricting

means/interface circuit 14 (Fig. 1) or 24 (Fig. 2) for restricting voltage transmitted from first internal circuit 12 to second internal circuit 16, thus anticipating each of claims 1 and 32. First MOS transistor 12 has a relatively thick gate insulation layer THICK OXIDE, and second MOS transistor 16 has a relatively thin gate insulation layer THIN OXIDE. Since the restricting means will restrict the voltage transmitted from first internal circuit 12 to second internal voltage 16, the electric field applied to the gate insulation layer of second MOS transistor 16 will be reduced, and claims 2 and 33 are anticipated. Power supply voltage VCC is an external power supply voltage, and the second voltage (i.e. ground) is lower than power supply voltage VCC. Therefore, claim 3 is anticipated. Interpreting Fig. 1 in a different manner, a power terminal (between 12 and 14) receives first high voltage VCCP when first transistor 12 conducts, wherein first transistor 12 has a drain coupled to the power terminal, a source coupled to first high voltage VCCP, and a gate coupled to a first input signal (that alternates between VCCP and 0V); second transistor 14 has a drain coupled to the power terminal, a gate coupled to second low voltage VCC lower than first high voltage VCCP, and a source coupled to a drain of third transistor 16, which has its source coupled to ground voltage, and a gate coupled to a second input signal (that alternates between VCC and 0V). Since first transistor 12 has a relatively thick gate insulation layer THICK OXIDE, and second/third transistors 14/16 each have a relatively thin gate insulation layer THIN OXIDE, claim 10 is anticipated. Since power supply voltage VCC is the second low voltage, claim 11 is also anticipated. The first input signal is selectable as one of a high level of first high voltage VCCP and a low level of ground voltage 0V, anticipating claim 12. The second input signal is selectable as one of a high level of second low voltage VCC and a low level of ground voltage 0V, anticipating claim 13. Interface circuit 14 has third MOS

transistor 14 with a relatively thin gate insulation layer THIN OXIDE, and the voltage from first MOS transistor 12 is applied to second MOS transistor 16 through third MOS transistor 14, anticipating claims 34-35. Since third MOS transistor 14 prevents first voltage VCCP from being directly applied to the drain of second MOS transistor 16, it enables second MOS transistor 16 to have the relatively thin gate insulation layer THIN OXIDE. Therefore, claim 36 is anticipated. Also, due to the voltage drop across third MOS transistor 14, the gate-drain voltage of second MOS transistor 16 will be effectively reduced to alleviate the electric filed applied to the gate insulation layer of second MOS transistor 16, anticipating claim 37.

Claims 19-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Wright et al. (Wright). Fig. 19 shows a semiconductor integrated circuit device comprising power terminal 222 receiving first high voltage VIO higher than power supply voltage VCORE of the device (e.g. see column 3, lines 48-57); first MOS transistor 210; second MOS transistor 212, third MOS transistor 206; fourth MOS transistor 208; fifth MOS transistor 202; sixth MOS transistor 204; and ground voltage 226. Since this Fig. 19 closely corresponds to the applicant's own Fig. 4, and the figure does not label the internal nodes, one of ordinary skill in the art would know the device also comprises the first-fourth internal nodes, thus anticipating claim 19. Wright discloses first/second MOS transistors 210/212 have a thick gate oxide; fifth/sixth MOS transistors 202/204 have a thin gate oxide; and third/fourth MOS transistors 206/208 can have a medium gate oxide (e.g. see column 4, lines 4-27). Since transistors with a medium gate oxide have relatively thin gate insulation layers with respect to those transistors with a thick gate oxide, claim 20 is anticipated. Power supply voltage VCORE is an internal power supply voltage of the device (e.g. see column 3, lines 49-50), and second low voltage VCORE is the power supply

voltage. Therefore, claim 21 is anticipated. First MOS transistor is controlled by a voltage of the second internal node (i.e. the node between 212 and 209), and second MOS transistor 212 is controlled by a voltage of the first internal node (i.e. the node between 210 and 206), anticipating claim 22. The gates of third/fourth MOS transistors 206/208 are coupled to second low voltage VCORE, which is lower than first high voltage VIO, thus anticipating claim 23. Power supply voltage VCORE is an internal power supply voltage of the device (e.g. see column 3, lines 49-50), and second low voltage VCORE is the power supply voltage. Therefore, claim 24 is anticipated. Fifth/sixth transistors 202/204 are controlled by first input signal VIN and its inverted version (via inverter 214), respectively, thus anticipating claim 25. It is understood that first input signal VIN, and its inverted version, are selectable to have one of a high level of second low voltage VCORE and a low level of ground (e.g. see column 3, lines 48-50; and the connection of inverter 214 between VCORE and ground), anticipating claim 26.

No claim is allowable as presently written.

***Allowable Subject Matter***

However, claims 4, 7, and 27-28 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art references to ensure: 1) the second MOS transistor is controlled by a row address signal in a memory device as recited within claim 4; 2) the third MOS transistor is controlled by a row address signal in a memory device as recited within claim 7; and 3) the first input signal includes a row address signal and a block selecting signal from a memory device as recited within claim 27, upon which claim 28 depends.

Also, claims 5-6, 8-9, 14-18, and 29-31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Claims 5-6 depend on objected to claim 4; claims 8-9 depend on objected to claim 7; and there is presently no strong motivation to modify or combine any prior art reference to ensure: 1) the second input signal includes a row address signal from a memory device as recited within claim 14, upon which claims 15-16 depend; 2) a fourth transistor, having a thin gate insulation layer, is coupled between the third transistor and ground as recited within claim 17, upon which claim 18 depends; and 3) the row decoder and drive block includes the row decoder and driver circuits as recited within claim 29, upon which claims 30-31 depend.

***Prior Art***

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although not used in any formal rejections described above, all three of these references show and disclose devices comprising at least three transistors coupled in series between a high voltage and ground, wherein at least one transistor coupled directly to the high voltage has a thick gate oxide, and at least one transistor coupled directly to ground has a thin gate oxide. For example, see Chang et al. (Fig. 3), Wert (Fig. 2), and Ha (Fig. 2). These figures also show a device with the first-sixth transistors corresponding to those recited in the present application's claim 19. Therefore, these references should be carefully reviewed and considered.

The prior art reference cited on the IDS submitted May 12, 2005 has been reviewed and considered. Although the reference of Lu et al. does disclose a thicker gate oxide with respect to

a pass transistor within a DRAM, and logic circuits with thinner gate oxides, the reference does not clearly show or disclose a device comprising the first/second MOS transistors and restricting means as recited within claim 1; the first-third transistors as recited within claim 10; the first-sixth transistors as recited within claim 19; or the first/second internal circuits and interface circuit as recited within claim 32.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

9 February 2006

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